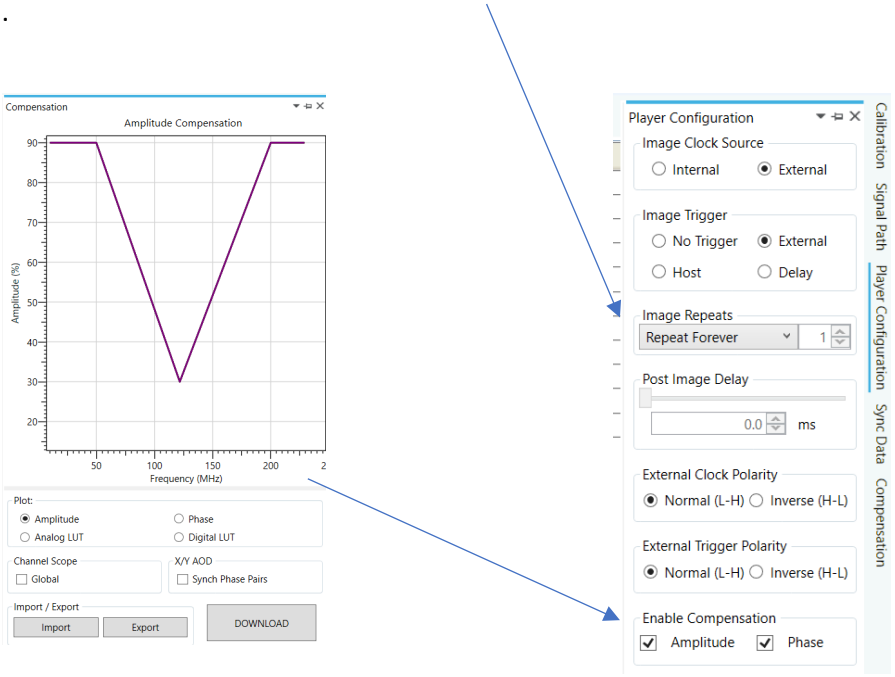
Input / Output Timing and Programmable Delays, rev-D.

- A user programmable delay can be applied between the Image clock and the RF output channels 1..4 on iMS4 outputs J1..4.
- A user programmable delay can be applied between the Image clock and the SDIO outputs on J7.

The programmable delay features aids synchronization particularly when the laser repetition rate approaches the acoustics fill time of the AOD deflectors.

The delay features are demonstrated below showing both C++ and GUI examples.

To aid illustration, a non-typical 'V' profile LUT amplitude file is loaded, and the Image Point amplitudes alternate between two values. ***Image Repeat*** should be set to ***Repeat Forever*** (see page 3).



Notes:

- Channel scoped Compensation table is applied.

- To replicate an X-Y deflector application, the Image data is programmed as follows:
  Frequency: Ch1 = Ch2, Ch3 = Ch4, and Ch1 ≠ Ch3
  Amplitude: Ch1 = Ch2, Ch3 = Ch4, and Ch1 ≠ Ch3

- External Trigger at ~3KHz

- External Clock, as noted below.

- SDIO digital sync data outputs on J7 are <u>inverted</u> with respect to the Image file data value.

  Bits-0…11 support < 2.5MHz Image data rates

- Two example Images are used, 10 and 26 points. In both cases the last point is set to 0% amplitude to give an "RF Off" terminating point.

Specifically:

Ch1, Ch2	Active range; 100-140MHz, max amplitude = 100%, low amplitude = 10%, "Off" amplitude; 0% set with a frequency of 90MHz
Ch3, Ch4	Active range; 95-135MHz, max amplitude = 60%, low amplitude = 50%, "Off" amplitude; 0% set with a frequency of 85MHz

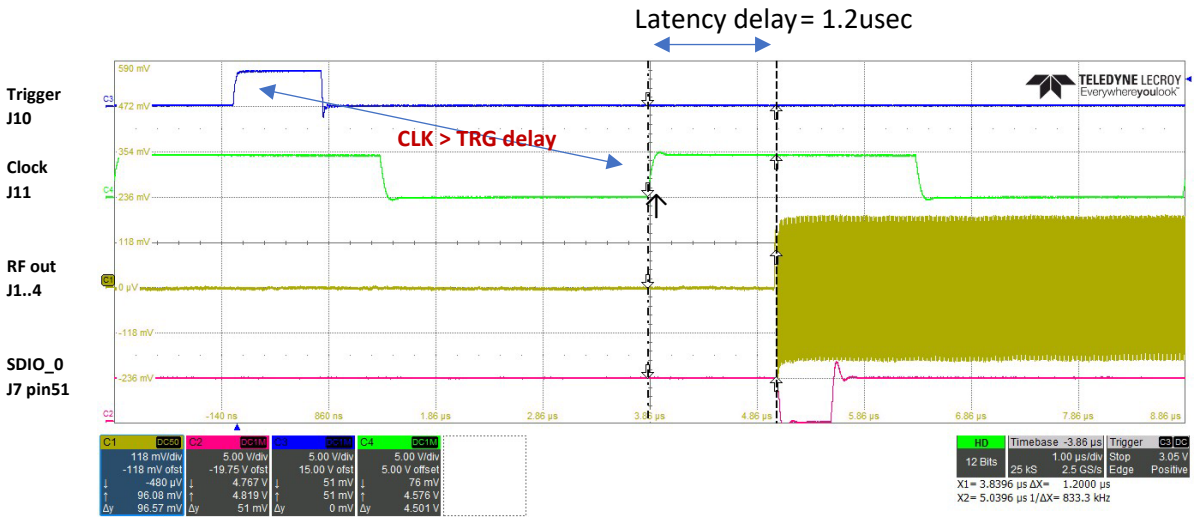
Default positive edge active is selected on external clock and trigger inputs.

IN ALL MODES:
There is a static latency (or pipe-line) delay of ~1.2usec between the external clock input edge and the corresponding Image point output, irrespective of the clock rate.

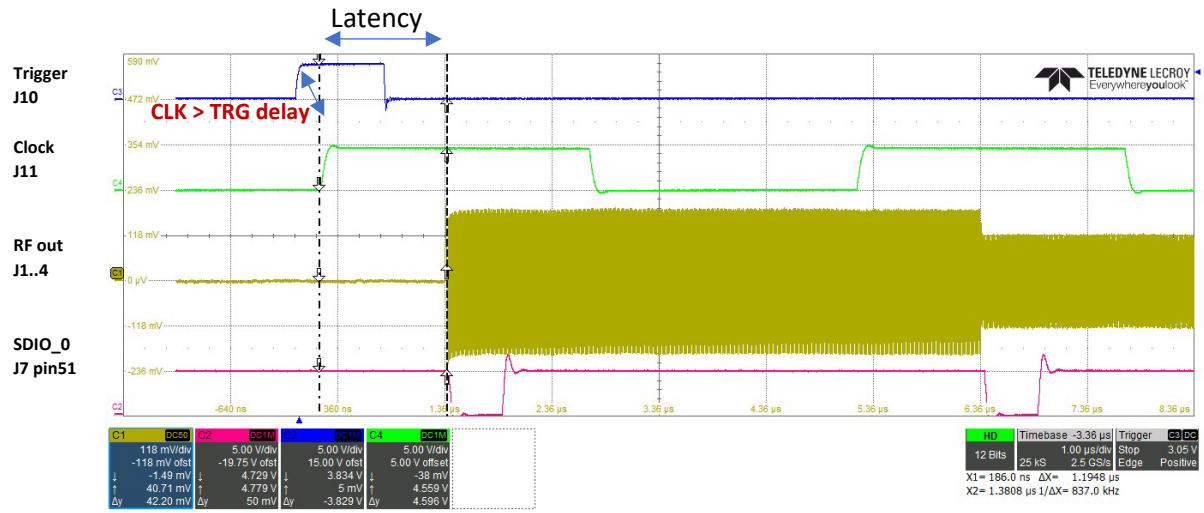
In the plots below.' ↑' indicates the first active clock edge after a valid external trigger.

1: External Trigger and Clock relative timing

The first Image point is output after the first clock edge (J11) following a valid trigger signal (J10).
In the trace below, SDIO is active. 500nsec ***Digital Sync Pulse Length*** and zero SDIO ***Output Delay.***



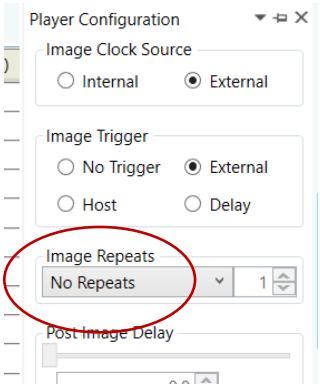
CLK > TRG delay : time delay between external trigger and clock edge is not critical



1.1 External Trigger > Output Jitter

Trigger to output update jitter = one Image (external or internal) clock period

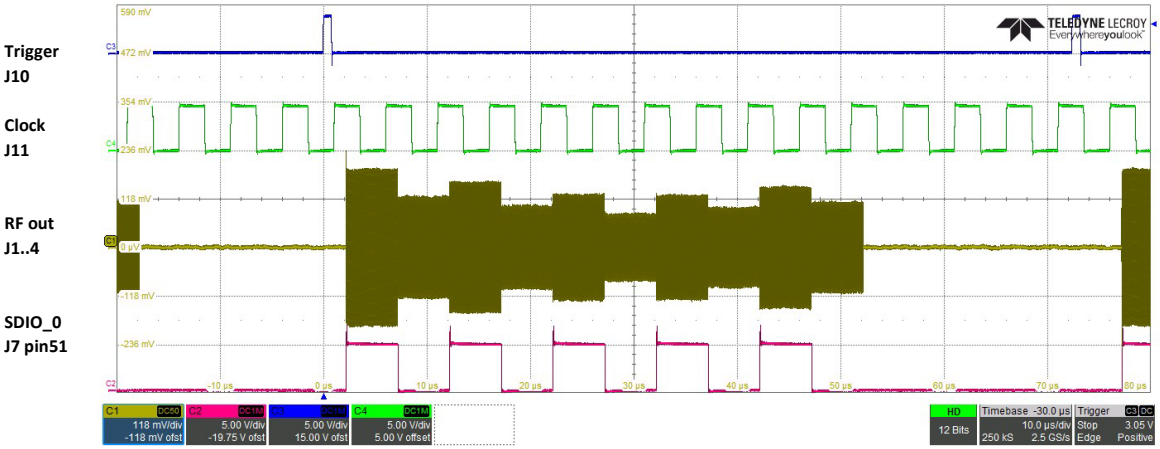
2: Image Repeats



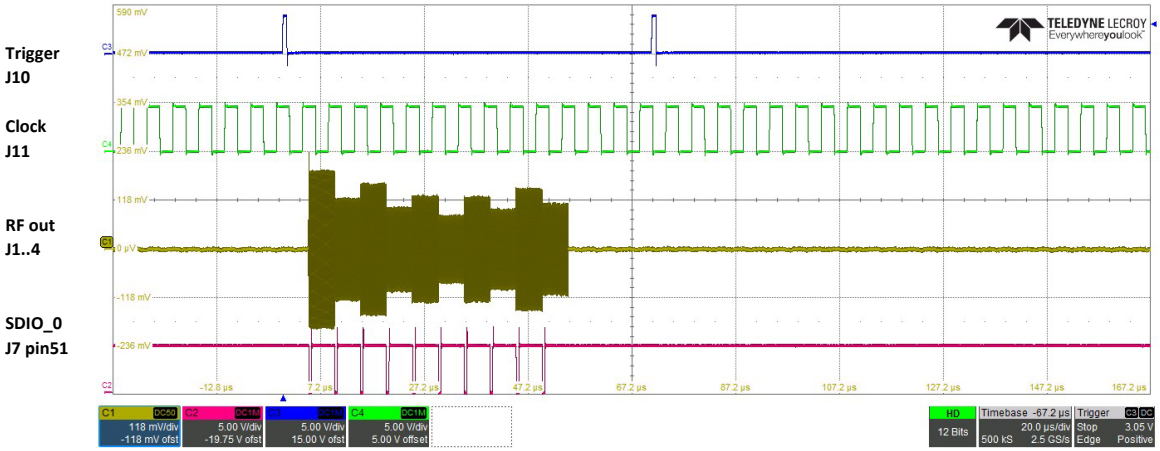
Typical case ***Image Repeats*** is set to ***Repeat Forever***

When ***Image Repeats*** is set to ***No Repeats***, then ONLY a single image is output per ***PLAY*** regardless of the number of subsequent triggers.

Case: Repeats



Case: No Repeats



3: **Limiting case, minimum Image size**

Image mode operation was originally designed for Image files containing >16 images points. However, with care, Image files down to >2 points can be used.

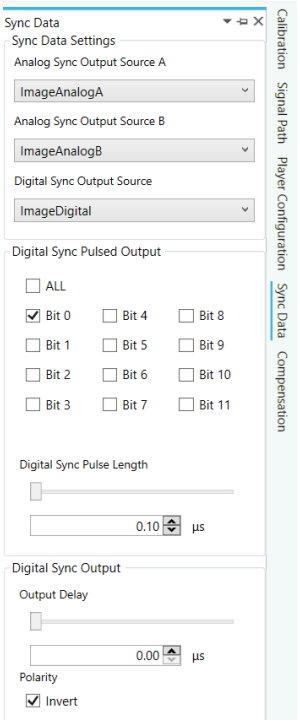
Enhanced Tone | 10pnt test | 2pnt test

	Ch1 Frequency (MHz)	Ch1 Amplitude (%)	Ch2 Frequency (MHz)	Ch2 Amplitude (%)	Ch3 Frequency (MHz)	Ch3 Amplitude (%)	Ch4 Frequency (MHz)	Ch4 Amplitude (%)	Sync Data (Dig)
▸	90.0000	100.0000	90.0000	100.0000	90.0000	100.0000	90.0000	100.0000	0x0FFF
1	140.0000	60.0000	140.0000	60.0000	140.0000	60.0000	140.0000	60.0000	0x0FFF

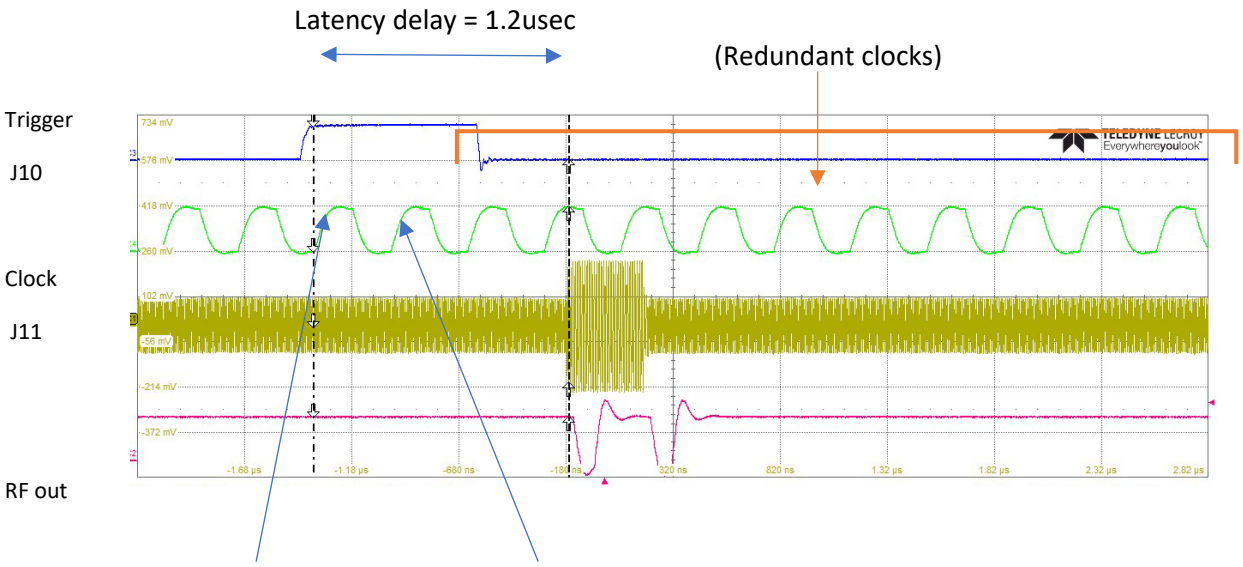
Consider one extreme example:

External clock (J11) = 2.8MHz
For reliable operation the
maximum external trigger rate (J10) = ~200KHz

SDIO set for Digital Sync Pulsed Output



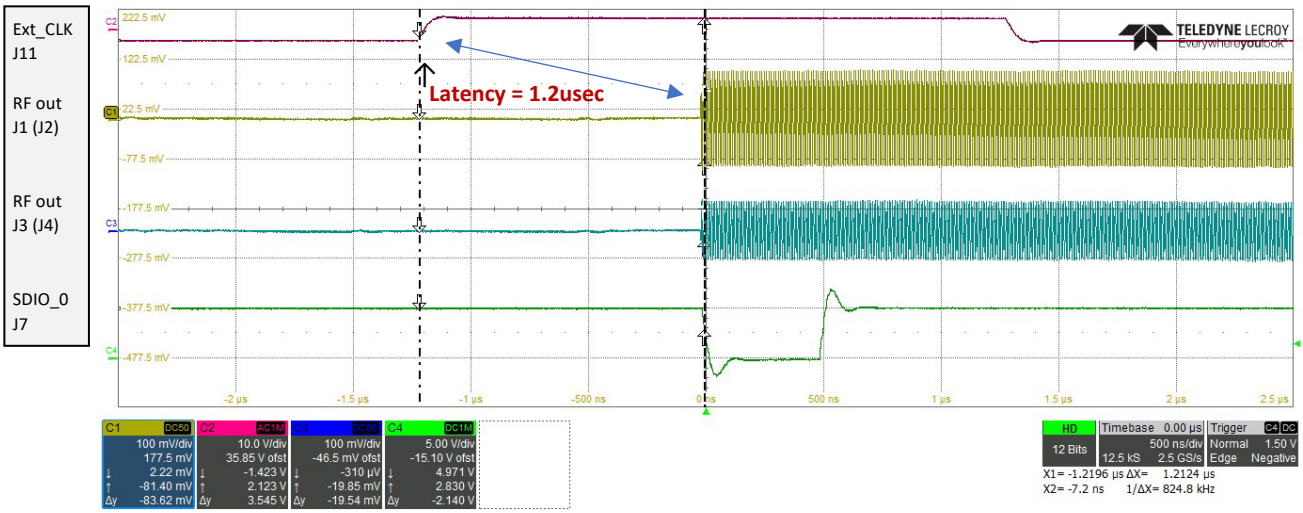
In this 2-point example. there is no termination image point with zero amplitude. The IMS4 continues to output the last image point frequency and amplitude until after the next trigger.



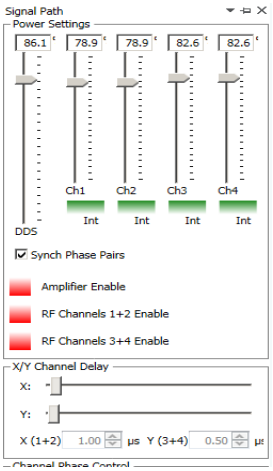
4: RF Output Channel Delay

- **Latency or Pipeline Delay. All programmable delays = zero**

Condition: Pulsed enabled SDIO; pulse width 500nsec, SDIO delay = 0nsec



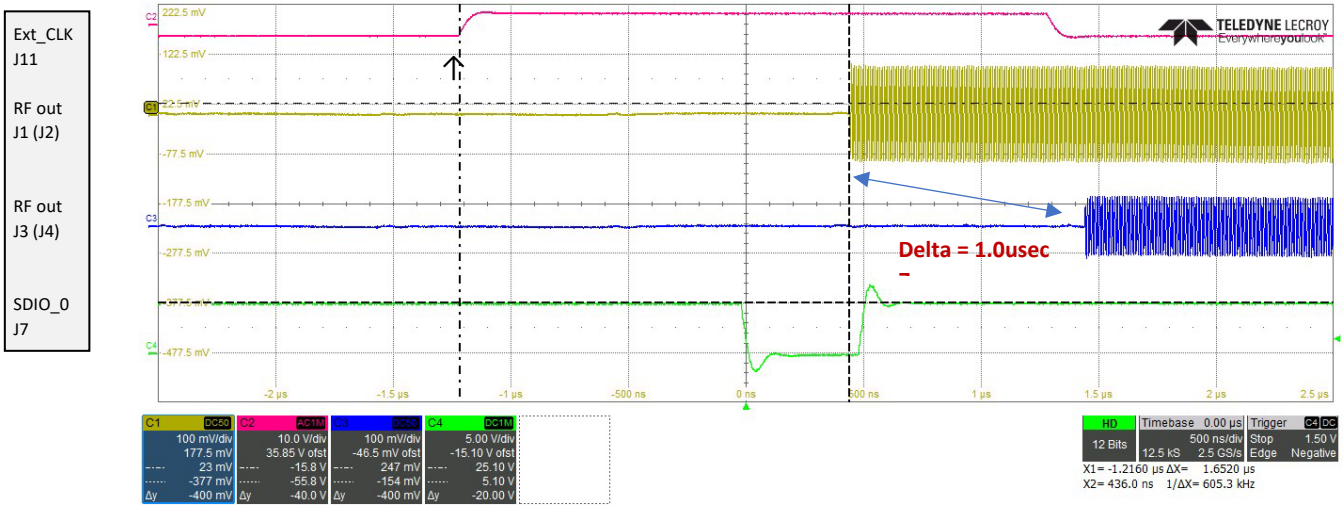
- **External Clock > RF Output Channel Delay**



In the Isomet GUI, the RF output channel delay control is applied across channel pairs as shown right.
This is a common requirement for X-Y AO beam-steered deflectors, where Ch1+2 (J1/J2) drives the X-axis, Ch3+4 (J3/J4) drives the Y-axis.

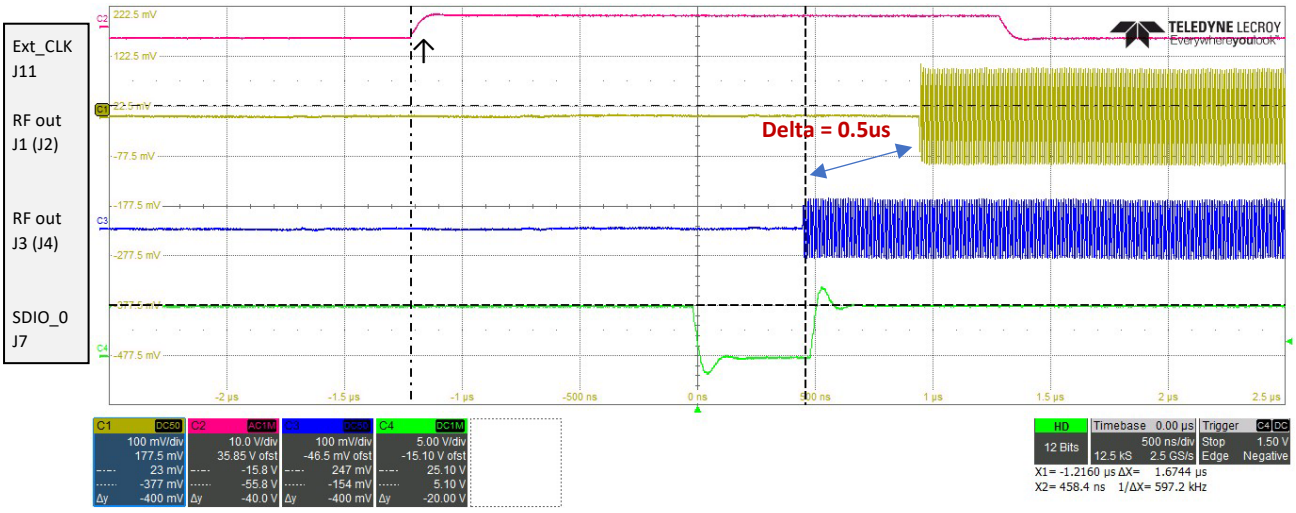
Condition: Ext-clock rate 200KHz. SDIO delay = 0nsec

A: Excluding latency delay, programmed with:
Clock to RF output channel delay on J1 = 500nsec
Clock to RF output channel delay on J3 = 1500nsec
Difference = +1000nsec



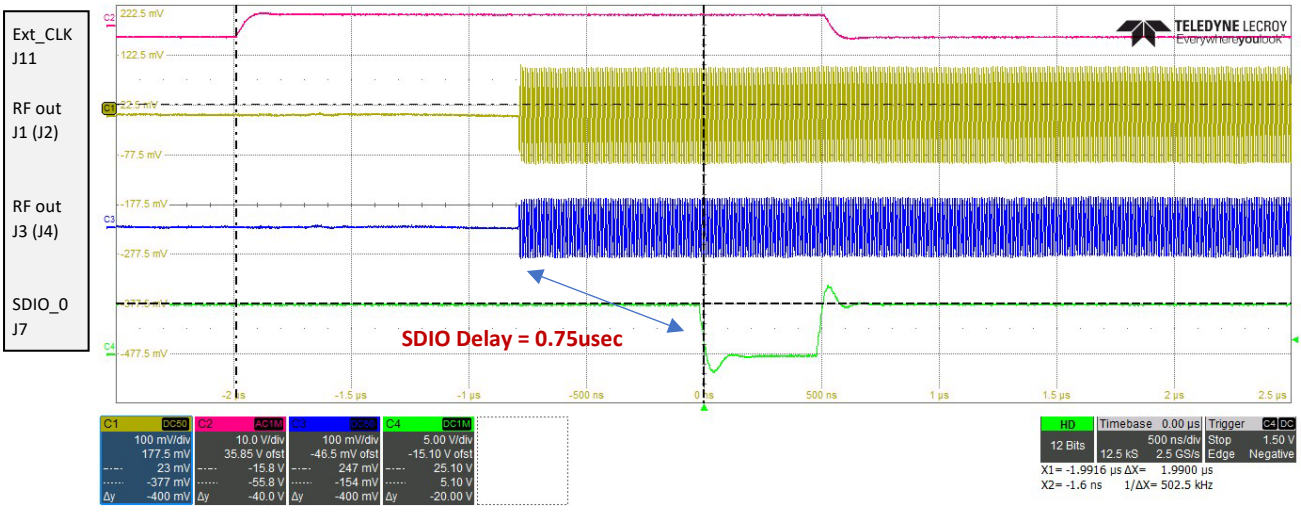
Condition: Ext-clock rate 200KHz, SDIO delay = 0nsec.

B: Excluding latency delay, programmed with:
Clock to RF output channel delay on J1 = 1000nsec
Clock to RF output channel delay on J3 = 500nsec
Difference = - 500nsec



5: External clock > SDIO Output Delay

Condition: Ext-clock rate 200KHz, RF output channel delay = 0nsec.
Excluding latency delay, programmed with:
Clock to SDIO output delay = 750nsec



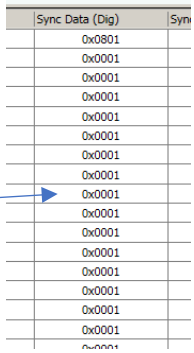
Next section describes SDIO characteristics in more detail

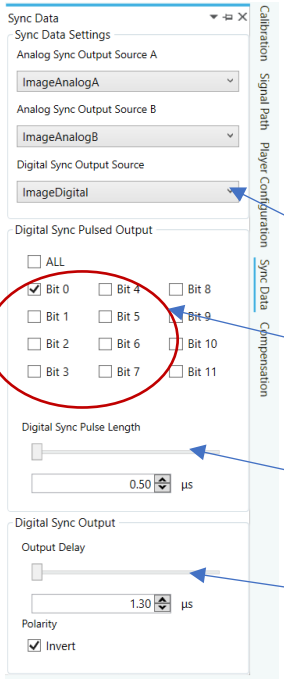
6: Sync Outputs J7

The default is level mode. ‘Level’ means the logic remains at constant state for the duration of the image point.

Unlike previous iMS4 build revisions, rev-D allows mixed SDIO output modes. Individual bits can be set for pulsed output.

Example: Bit-0 is programmed for pulsed on all points = 0x0001.
Bit-11 programmed for level, first Image point only = 0x0801





Polarity Inverted (default)
Data bit high = low at J7 output

`

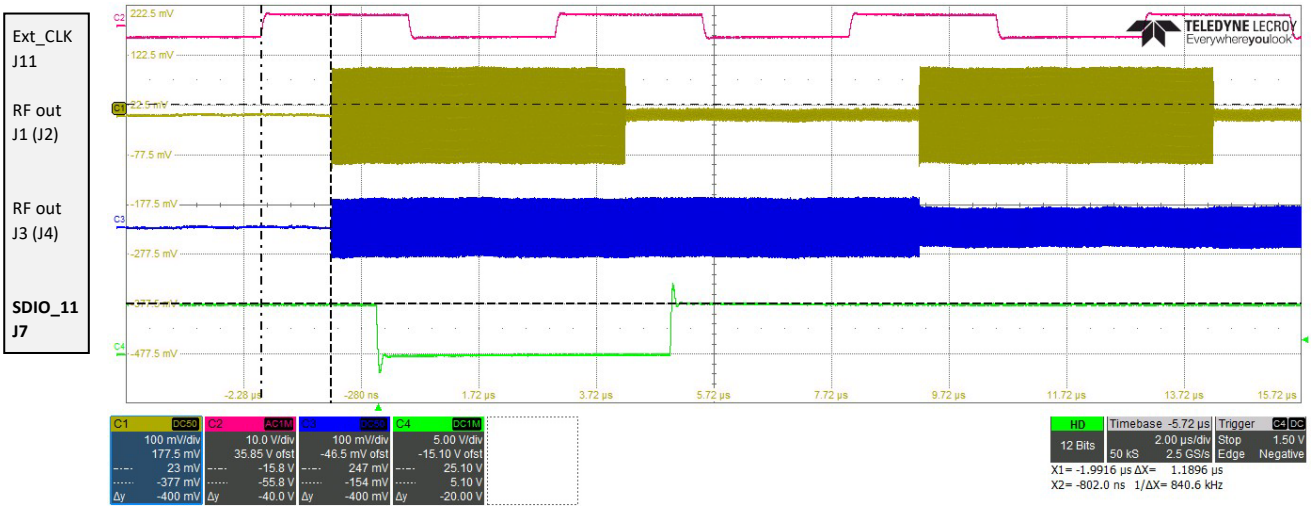
To generate a pulse output per image point:
Select source = *ImageDigital*

CHECK the *Digital Sync Pulse Output* box(es) on required bits.

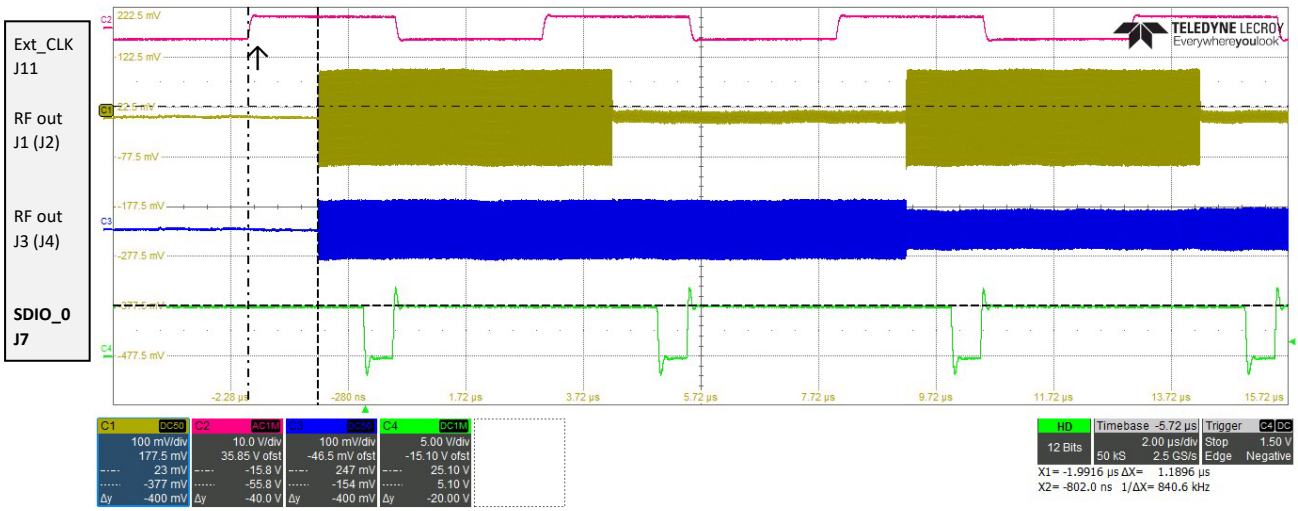
Input a ***Digital Sync Pulse Length*** (usec)
MUST be less than external clock period.

Input a ***Digital Sync Output Delay*** (usec)
MUST be less than external clock period.

Condition: Ext-clock rate 200KHz, RF output channel delay = 0nsec.
Programmed with SDIO bit 11 = level, SDIO Output Delay = 0.75usec (not 1.3 as shown above)

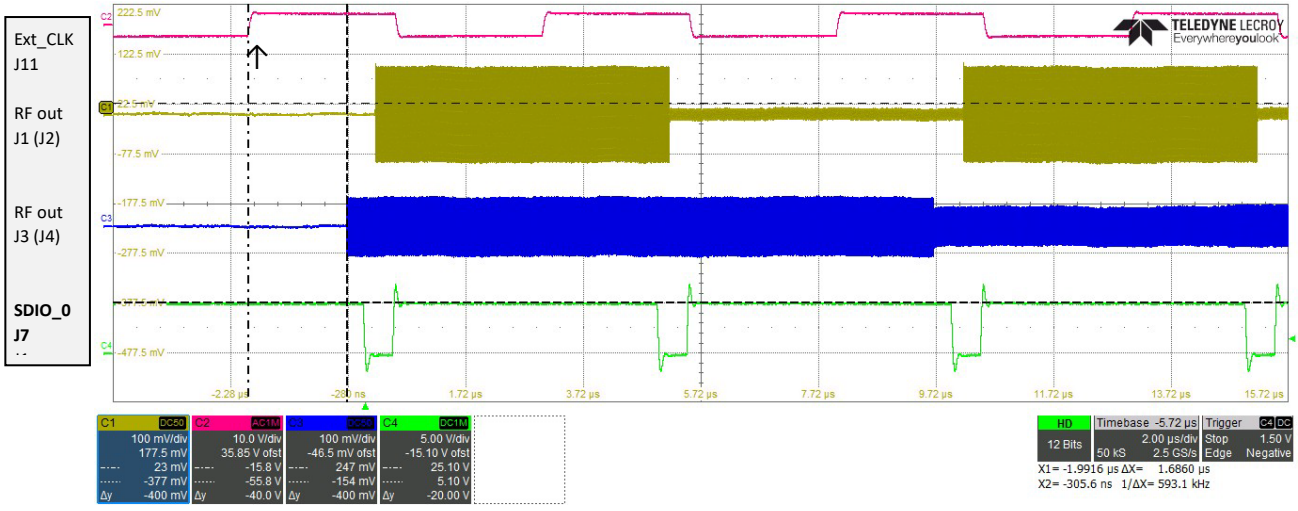


Condition: Ext-clock rate 200KHz, RF output channel delay = 0nsec.
Programmed with SDIO bit 0 = pulsed, SDIO pulse width 0.5usec, SDIO delay = 0.75usec



Note: the fixed 1.2usec latency from rising clock edge ↑ to the active RF output, (no programmed Channel or RF delay)

As above, and programmed with RF output channel 1+2 delay = 1000nsec,
channel 3+4 delay = 500nsec.



7: Associated C++ code, SDK v1.8.9

RF Channel delay

```
SignalPath sp(*myiMS);

int Dly12, Dly34; // delay value First ch pair, Second ch pair
sp.SetChannelDelay(std::chrono::nanoseconds(Dly12), std::chrono::nanoseconds(Dly34));
```

SDIO configure and delay

```
std::chrono::nanoseconds SyDly(000);      // define pulsed SDIO delay
std::chrono::nanoseconds PW(200);         // define pulsed SDIO pulse width

SignalPath SDOR(*myiMS);

SDOR.AssignSynchronousOutput(SignalPath::SYNC_SINK::DIG,
                                                SignalPath::SYNC_SRC::IMAGE_DIG);

// Rev-D bit configurable pulse or level SDIO
SDOR.ConfigureSyncDigitalOutput(SyDly, PW); // enable pulsed SDIO (delay, width)

SDOR.SyncDigitalOutputMode(SignalPath::SYNC_DIG_MODE::LEVEL,11); // enable level SDIO
                                                                    for bit 11 only
```

8: Note: Maximum 2.5MHz rate SDIO output rate

2023-10-31 We have identified an issue with SDIO output when operating at Image clock rates above 2,5MHz, especially when the SDIO is programmed to change frequently within an image . This does not affect the RF outputs, which are still Ok up to the maximum of 3.5MHz.

- If the SDIO is not performing a critical function, this limitation may not be an issue.
- Depending on the application and how the SDIO is programmed, there may be few/no errors, but not with certainty.
- Increased rates are expected in future fireware releases. All revD firmware is field programmable.